

Power Circuit Technology using Next-generation SiC Power Semiconductors for Power Electronics Devices in Electric Powertrain

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ABSTRACT

Next-generation silicon carbide (SiC) power semiconductors are expected to offer size reductions and increased efficiency. Optimized design is necessary for the power circuits employing these semiconductors in order to exploit their performance potential. The identification of each circuit element related to transient response during high-speed switching, a characteristic of SiC power semiconductors, and the correlation of circuit simulation models with the results of actual measurements, made it possible to obtain voltage and current waveforms to within a 4% level of error.

Using this circuit simulation technology, the most important circuit elements to power circuit design were identified. The employment of optimized values in sections of the circuit in which parasitic impedance affected efficiency and electromagnetic interference (EMI) performance was shown to reduce switching loss and noise.

1. Introduction

With the transition to the use of higher levels of power, it becomes necessary to make the power electronics devices such as inverters and converters used in electric vehicles and similar vehicles smaller, more efficient, and less prone to electromagnetic interference (EMI). Power semiconductors are one of the key technologies employed in power electronics devices. Most semiconductors today are based on silicon (Si), but the performance limits of the material have been reached, and research and development efforts are proceeding in the area of SiC semiconductors, a type of next-generation power semiconductor expected to offer ultra-low levels of loss. However, because SiC power semiconductors are capable of high-speed switching, they present issues with regard to their use in automotive applications, including reduced efficiency and increased EMI, making optimal power circuit design essential.

Parasitic impedance in power semiconductor chips, electrical wiring, and other components is an important parameter in realizing faithful reproduction of circuits by the circuit simulation technologies used at the design stage. The development of a circuit simulation technology that reflected this parameter would make it possible to (1) simulate a power circuit able to reproduce the high-speed switching operation of an SiC power semiconductor, and (2) analyze and evaluate the voltage and current when EMI originating in high-speed switching by an SiC power

semiconductor occurs.

This paper discusses the development of a circuit simulation that reproduces the high-speed switching operation of an SiC power semiconductor, the identification of areas of circuits with a significant effect on EMI due to voltage and current waveforms, and achieved noise reduction results. The achievement of good reproduction of voltage and current waveforms was an important factor in realizing this development, in respect of their relationship to loss in devices and the efficiency of the system as a whole.

2. SiC Power Semiconductors: Characteristics and Issues of Application

Figure 1 shows the theoretical limit line for the on-resistance of Si and SiC. As this graph indicates, a dramatic increase in on-resistance performance can be expected from the use of SiC against Si.

To provide an indication of projected performance increases, Table 1 shows a comparison of the characteristics of new semiconductor materials with those of the conventionally used Si⁽¹⁾.

On-resistance, $R_{on}A$, an important parameter for power semiconductors, can be expressed by Eq. (1)⁽²⁾.

$$R_{on}A = \frac{4V_B^2}{\mu\epsilon E_c^3} \quad (1)$$

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Table 1 Comparative characteristics of new semiconductor material and Si

Material Physicality	New semiconductor			Conventional semiconductor
	SiC (4H)	Diamond	GaN	Si
Breakdown strength (10^6 V/cm)	2.5	10.0	3.3	0.3
Energy bandgap (eV)	3.26	5.47	3.39	1.12
Electronic saturation velocity (10^7 cm/s)	2.2	2.7	2.7	1.0
Thermal conductivity (W/cm·K)	4.9	20.9	2.0	1.5
Stage of wafer manufacturing technology	Mass production in part	Research	Development	Mass production

V_B : Breakdown voltage

μ : Bulk migration

ε : Permittivity

E_c : Breakdown strength

From Eq. (1), $R_{on}A$ is inversely proportional to the cube of E_c . Because the E_c of new semiconductor materials is at least eight times that of Si, as shown in Table 1, it is possible to expect that the use of these materials will help enable chips to be reduced in thickness, thus reducing on-resistance.

The use of insulated gate bipolar transistors (IGBT), which are unipolar and bipolar compound devices and make it possible to realize higher withstand voltage than in the case of unipolar metal oxide semiconductor field-effect transistors (MOSFET), is common in the field of high withstand voltage power semiconductors. Employing high withstand voltage SiC power semiconductors will make it possible to use unipolar device configurations, helping to enable high-speed switching.

Diamond and GaN display a similar level of potential to SiC as next-generation semiconductor materials. However, in terms of the stage of advancement of wafer manufacturing technology, wafers using diamond materials are still at the research stage and wafers using GaN materials are under development, while wafers using SiC materials are at the stage of partial mass production. At present, therefore, the highest expectations are on devices using SiC.

However, some issues arise in the application of SiC power semiconductors. Because SiC is capable of realizing high-speed switching, increases in voltage and

current surges and ringing and common mode current due to parasitic impedance make it a challenge to adequately exploit the high performance of which SiC is capable. The design of power circuits that are optimized for the complete vehicle is important in responding to these issues, and this makes a circuit simulation technology able to be applied to the development and analysis of optimal power circuits essential.

3. Circuit Simulation Technology

In order to formulate circuit simulation models, the research discussed here selected SiC power MOSFET and Schottky barrier diodes (SBD), which can be applied in hybrid, electric, and similar vehicles, for the power semiconductor chip configuration. Figure 2 shows the graphical symbols for each. Here, V_{ds} is the voltage between the drain and the source, I_d is the drain current, V_{gs} is the voltage between the gate and the source, V_f is the voltage between the anode and the cathode, and I_f is the anode current.

Figure 3 shows an example of circuits as employed in the powerplant system of an electric vehicle. Here, C_b is parasitic capacitance between the battery and the body, C_i is parasitic capacitance between the inverter and the body, C_l is parasitic capacitance between the three-phase line and the body, and C_m is parasitic capacitance between the motor and the body. For the simulation model system, a single-ended push-pull circuit of the type shown in Fig. 4, which forms the basis of devices including inverters and converters, was employed. C_i' is the parasitic capacitance determined by the SiC MOSFET/SBD power module configuration. With regard to common mode current, while parasitic capacitance exists between the body and all the components including

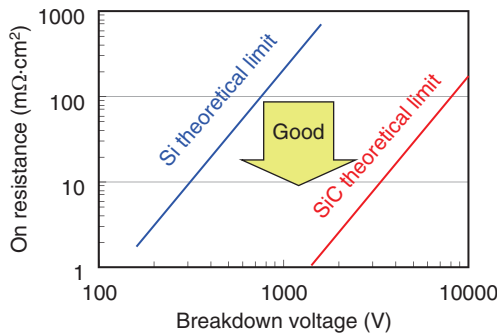


Fig. 1 Si and SiC theoretical limit line

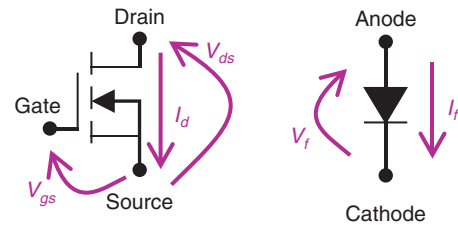


Fig. 2 MOSFET and SBD symbol

the motor, here, for the sake of simplicity, the parasitic capacitance between the body and the motor, the battery, and the three-phase line is summed, and the parasitic capacitance divided between PN is taken as C_0 , creating an equivalent circuit that makes it possible to conduct a comparative analysis of the effect of common mode current.

The flow of procedures for the circuit simulation technology is as follows:

- (1) Listing of circuit parameters
- (2) Fitting of models of power semiconductor chips
- (3) Calculation of parasitic impedance
- (4) Formulation of circuit model
- (5) Verification using results of tests

3.1. Listing of Circuit Parameters

Table 2 shows the parameters that are essential to the formulation of the circuit simulation. Figure 5 shows the capacitance parameters for the power semiconductor chips.

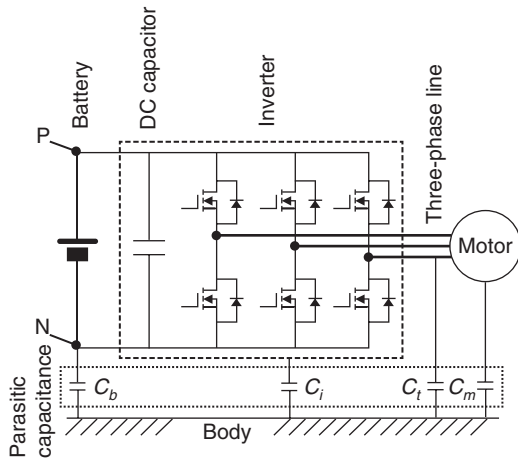


Fig. 3 System model

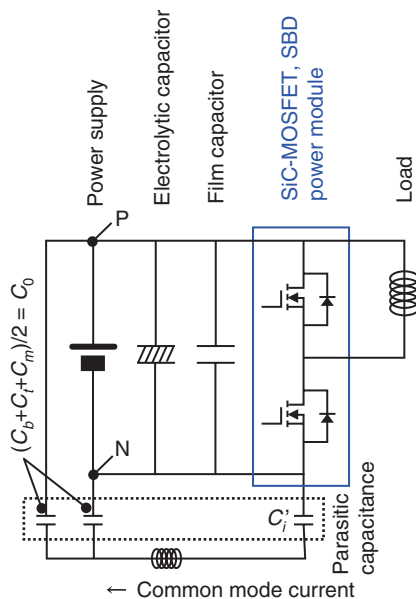


Fig. 4 Simulation model system

Table 2 Parameter list

Division	Subdivision	Parameter
Chip	SiCFET	I_d - V_{ds} Characteristic
		C_{dg} - V Characteristic
		C_{ds} - V Characteristic
		C_{gs} - V Characteristic
	SiCSBD	I_f - V_f Characteristic
Other parts	Bus bar	Parasitic inductance/resistance
	Electrode plate	
	Wire	
	Insulating substrate	Parasitic capacitance

C_{dg} is the capacitance between the drain and the gate, C_{ds} is the capacitance between the drain and the source, C_{gs} is the capacitance between the gate and the source, and C_{ac} is the capacitance between the anode and the cathode. The parameters listed are electrical characteristics (static and dynamic characteristics) for the chips and all parasitic impedance originating in the structural parts such as the bus bar for parasitic impedance.

3.2. Fitting of Models of Power Semiconductor Chips

The models of power semiconductor chips are fitted by setting the parameters so that the characteristics expressed by approximation equations closely match the characteristics determined by actual measurements.

3.2.1. SiC FET

(1) I_d - V_{ds} characteristic

The approximation equations for I_d are

$$I_d = I_{sat} (1 + \lambda \cdot V_{ds}) \left(2 - \frac{V_{ds}}{V_{sat}} \right) \frac{V_{ds}}{V_{sat}} \quad (2)$$

for the linear domain, and

$$I_d = I_{sat} (1 + \lambda \cdot V_{ds}) \quad (3)$$

for the saturation domain.

Here, the saturation voltage, V_{sat} , and the saturation current, I_{sat} , are expressed as

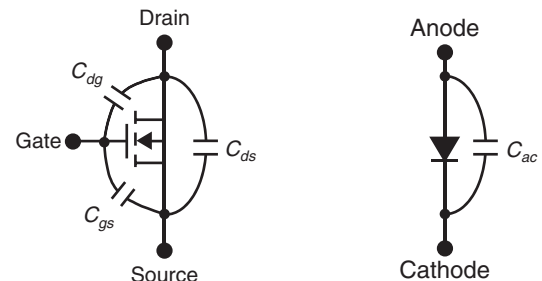


Fig. 5 Chip C parameter

$$V_{sat} = A(V_{gs} - V_p)^M \quad (4)$$

$$I_{sat} = \frac{K}{2}(V_{gs} - V_p)^N \quad (5)$$

λ : Channel length modulation parameter

V_p : Pinch-off voltage

K : Transfer conductance coefficient

A : Saturation voltage coefficient

M : Saturation voltage exponent

N : Saturation current exponent

Figure 6 shows the fitted I_d - V_{ds} characteristic with each parameter set.

(2) C - V_{ds} characteristic

The approximation equation for C is as follows:

$$C = C_c \left[\delta + \frac{1-\delta}{(1+V_{ds}/V_{Diff})^\alpha} \right] \quad (6)$$

C_c : Capacitance constant

α : Junction grading coefficient for C

δ : Junction correction factor for C

V_{Diff} : Diffusion voltage

Figure 7 shows the fitted C - V_{ds} characteristic with each parameter set.

3.2.2. SiC SBD

(1) I_f - V_f characteristic

The approximation equation for I_f is as follows:

$$I_f = I_{sat_fwd} \left[\exp \left(\frac{V_f}{M_{fwd} \cdot V_T} \right) - 1 \right] \quad (7)$$

M_{fwd} : Carrier correction value

I_{sat_fwd} : Operating point saturation current

R_{b_fwd} : Junction bulk resistance

V_T : Thermal voltage (25.5 mV in a 300 K environment)

Figure 8 shows the fitted I_f - V_f characteristic with each

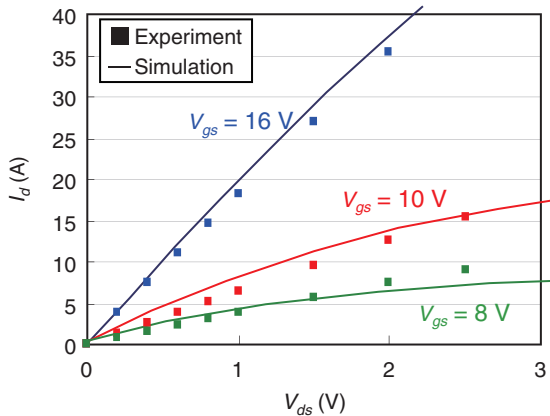


Fig. 6 I_d - V_{ds} fitting diagram

parameter set.

(2) C - V_r characteristic

The approximation equation for C is as follows:

$$C = C_{j0} \left[\delta + \frac{1-\delta}{(1-V_r/V_{Diff})^\alpha} \right] \quad (8)$$

C_{j0} : Zero bias junction capacitance

$V_r = -V_f$

Figure 9 shows the C - V_r characteristic with each parameter set.

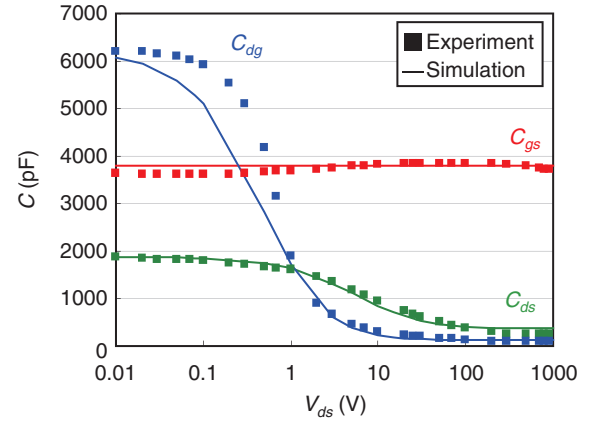


Fig. 7 C - V_{ds} fitting diagram

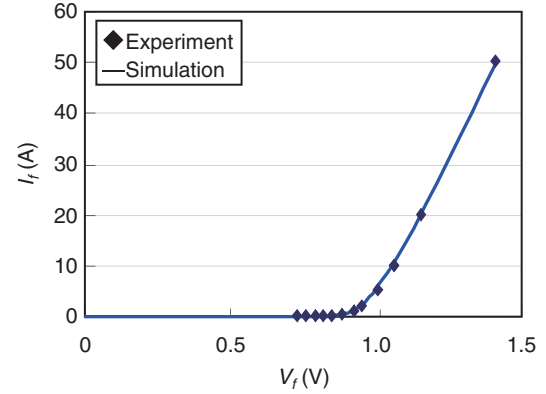


Fig. 8 I_f - V_f fitting diagram

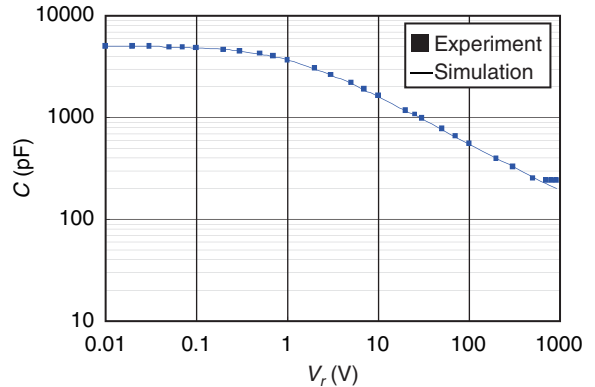


Fig. 9 C - V_r fitting diagram

3.3. Calculation of Parasitic Impedance

Figure 10 shows a diagram of the SiC MOSFET/SBD power module used in the simulation circuit model. The values of parasitic impedance for the constituent components of the module were determined using three-dimensional LCR parameter identification software, based on the configuration shown in Fig. 10. Here, parasitic inductance, a parameter with a strong relationship with surge voltage, was calculated with consideration of the mutual inductance generated by the overlapping of the current paths.

3.4. Formulation of Circuit Model

Equivalent circuit models were formulated by incorporating the power semiconductor chip models fitted in Section 3.2 and the parasitic impedances calculated in Section 3.3. In order to help ensure greater accuracy in reproduction, distributed constant models, as represented by C_1 and C_2 , were employed for the direct brazed copper (DBC) substrate model. Figure 11 shows a diagram of the circuit simulation.

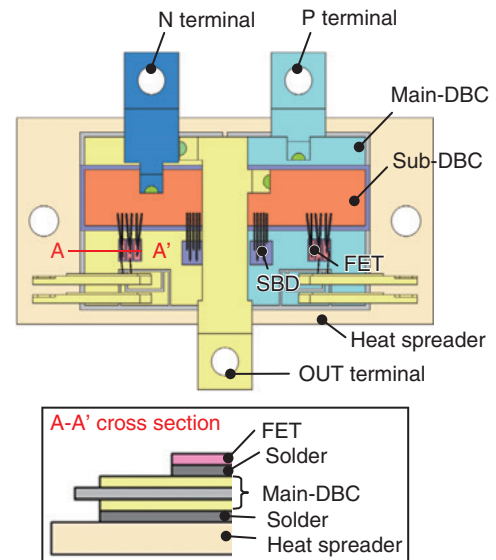


Fig. 10 SiC-MOSFET, SBD power module diagram

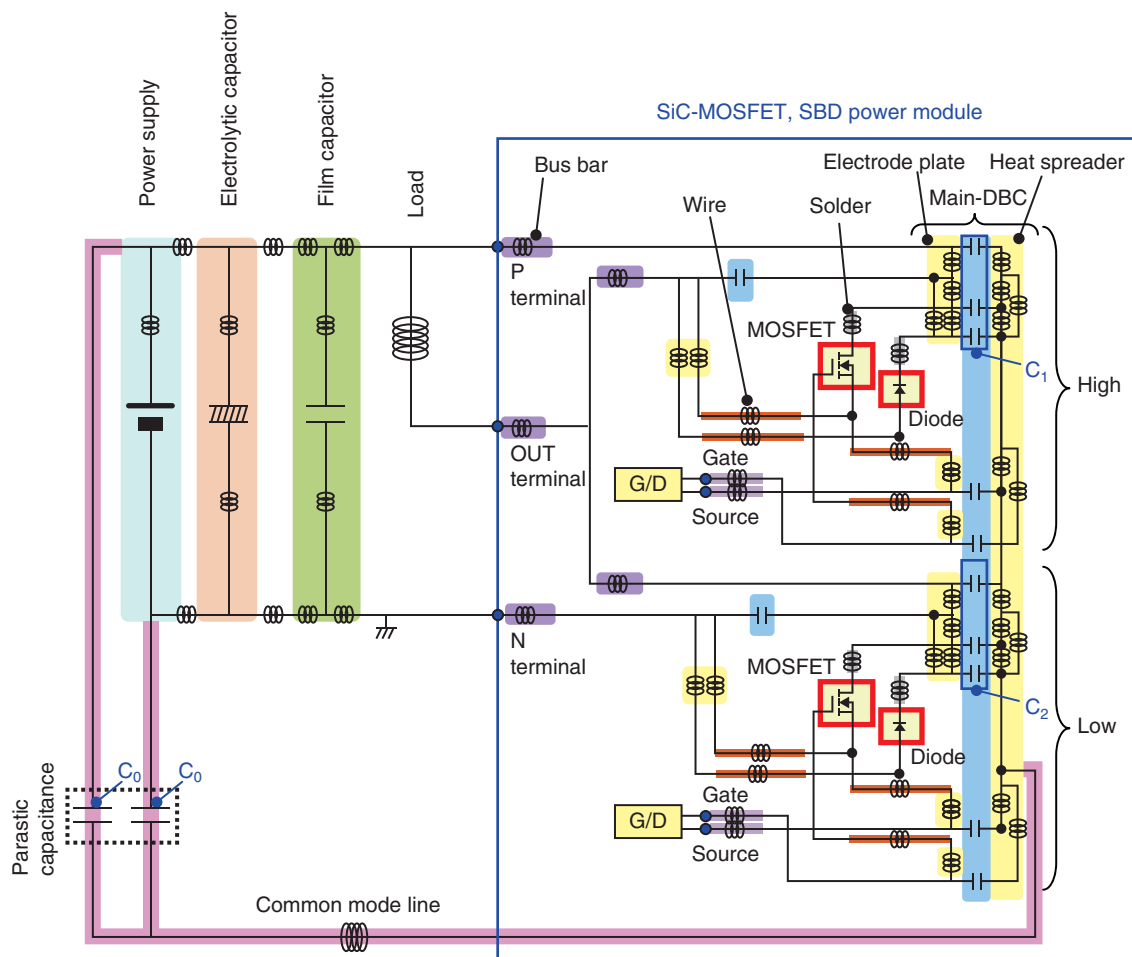


Fig. 11 Simulation diagram (resistance abbreviated)

Table 3 Comparison between experiment and simulation

				Gap
I_d (at turn on)	Peak (A)	Experiment	68	- 3 %
		Simulation	67	
	Frequency (MHz)	Experiment	11.2	+ 18 %
		Simulation	13.2	
V_{ds} (at turn off)	Peak (V)	Experiment	283	- 4 %
		Simulation	280	
	Frequency (MHz)	Experiment	26.3	- 39 %
		Simulation	18.9	

3.5. Verification using Results of Tests

Figures 12 and 13 respectively show the turn-on and turn-off waveforms for the SiC MOSFET. Table 3 shows the peak value for I_d and the ringing frequency at turn-on, and the peak value for V_{ds} and the ringing frequency at turn-off. The test conditions employed were a source voltage of 200 V and drain currents of 30 A (at turn-on) and 40 A (at turn-off).

Results were obtained for peak values of voltage and current within an error of 4% at both turn-on and turn-off. Results for ringing frequency were within 40% error, necessitating the realization of a greater degree of

correspondence in the model through correlation with parasitic impedance. However, because a match on the MHz order was obtained in the EMI analysis, qualitative judgments were considered possible, and the analysis proceeded using the developed circuit simulation.

4. Identification of Important Parts in Power Circuit and Results

Using the circuit simulation technology discussed in Chapter 3, a study was conducted to identify the circuit parameters in a power circuit network that are important in relation to EMI generated by resonance frequencies. These parameters were shown to be C_1 , C_2 , and C_0 in Fig. 11.

Figure 14 shows results for common mode noise obtained by optimizing these parameters. Common mode current increases by 12.8% in the case of an SiC MOSFET (without optimized design of constants) against a conventional Si IGBT, but optimized design of values reduces the figure for the SiC MOSFET by 81.8%. Figure 15 shows the common mode current waveforms for the circuits. Figures 16 and 17 compare normal mode noise and switching loss for the circuits. Because the SiC power semiconductor offers high-speed switching, normal mode noise increases by 125% against the Si IGBT element, but optimized design of constants results in a 41.5% reduction of noise. With regard to switching loss, results indicate that further reductions can be expected with optimized design of constants.

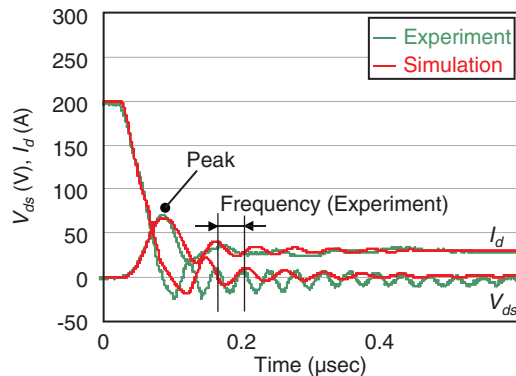


Fig. 12 Turn-on waveform

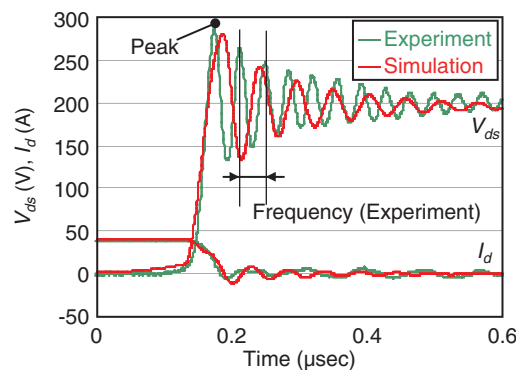


Fig. 13 Turn-off waveform

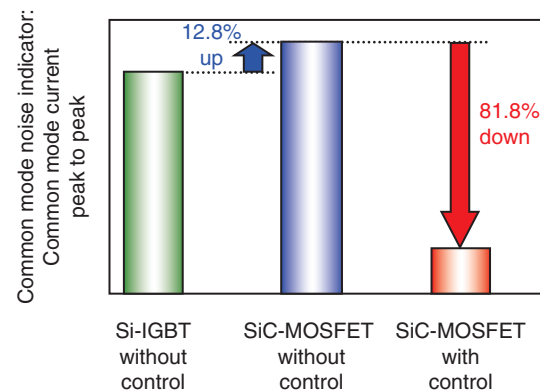


Fig. 14 Common mode current comparison

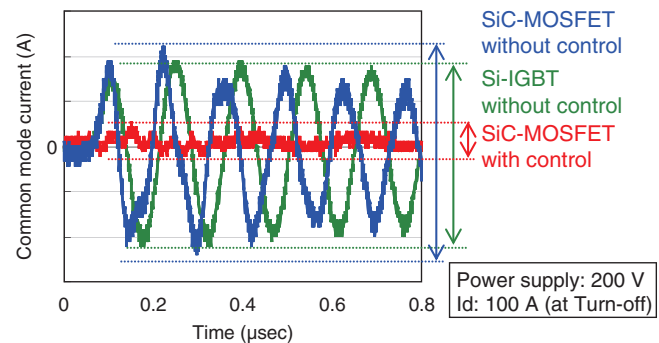


Fig. 15 Common mode current waveform

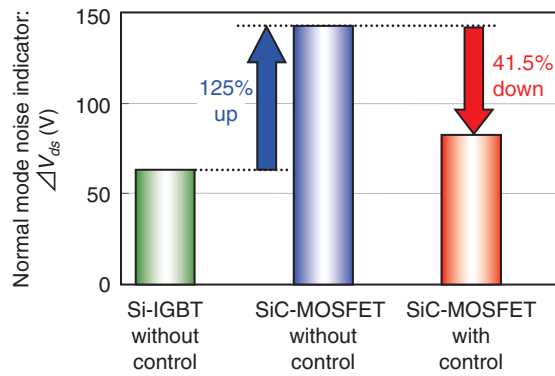
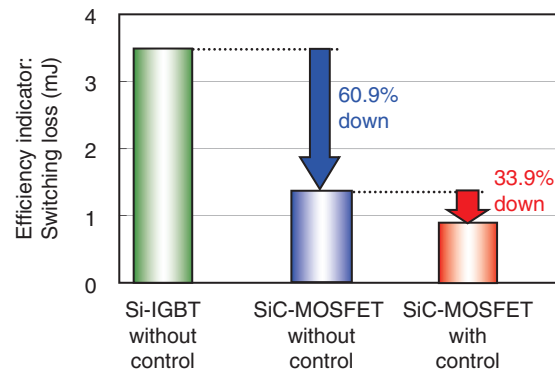
Fig. 16 ΔV_{ds} comparison

Fig. 17 Switching loss comparison

competitive power electronics devices. In future, in relation to EMI, it will be necessary to achieve further detailed correspondence of the parasitic impedance around the main interconnections related to normal mode noise.

References

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5. Conclusion

The development of a simulation technology for high-speed switching power circuits employing SiC power semiconductors produced the following results:

- (1) Three-dimensional LCR parameter identification software was used to determine power semiconductor chip parameters and parasitic impedance between the wiring and interconnections of structural parts; correlation with actual measurements and the further correction of parameters involved in mutual inductance helped to enable the setting of highly accurate power circuit parameters.
- (2) The results of correlation with voltage and current waveforms and frequencies and the evaluation of performance as power circuits indicated that figures for surge voltage and current error were within 4%. Using the circuit simulation technology described above, the following results were obtained for efficiency and EMI performance.
- (3) Circuit parameters closely related to efficiency and EMI performance were identified, and reductions of 81.8% in common mode noise and 33.9% in switching loss were achieved through optimized design of constants.

The results produced by the technology considered in this research indicate that the application of SiC power semiconductors will help enable the design of highly

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