

Time-sharing PWM Control for Multi-motor Drive

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ABSTRACT

The necessity for the use of multi-motor drive systems is increasing, for example in hybrid vehicles, fuel cell vehicles and electric vehicles. Multiple-output inverters, which are able to drive multiple motors simultaneously, are available as a means of preventing the system enlargement with the increase in the number of motors.

The project discussed in this paper applied time-sharing PWM control to a multiple-level multiple-output inverter. The viability of proposed control method was confirmed and power loss characteristics were clarified. Within the operating range in which the sum of the voltages supplied to the multiple motors did not exceed the voltage of the power source, an output current control characteristic equivalent to that of a conventional independent inverter was achieved. In addition, the project demonstrated that the use of switching devices with superior current conduction characteristics in the multiple-level system was an effective means of increasing efficiency.

1. Introduction

Demands for the reduction of environmental impacts by automobiles are increasing recently. Energy conservation technology by electric motor represents one means of responding to these demands. Efficient systems using three-phase motors are being employed as vehicle drive systems producing several tens of kW or more, as systems driving electric air conditioners producing several kW in hybrid and electric vehicles, and as systems driving electric power steering in large vehicles.

Figure 1 shows the conventional parallel configuration of the three-phase inverters that are necessary to drive

multiple motors. Three-phase inverters used for motor drive employ multiple power switching devices, and the number of switching devices should be reduced to lower costs and to reduce size. One means of reducing the number of switching devices is to employ multiple-output inverters that share some switching devices among multiple inverters. The circuit configurations of multiple-output inverters can be divided into multi-phase systems that reduce the number of phases by sharing phases [Fig. 2 (a)]^{(1), (2)} and multi-level inverter systems that use series-connected switching devices for each phase and share the some of the switching devices [Fig. 2 (b)]. A number of R&D projects are being conducted on multi-phase systems, but the number of components that can be reduced is small in the case of these systems, and they have not yet come into practical use. A type of multi-level system in which the carrier waveform is divided into several voltage levels has been proposed^{(3), (4)}. However, the detailed analyses of power conversion efficiency for multi-level inverters have not been conducted yet.

The research discussed here proposed the use of time-sharing PWM control for multi-level inverters. The proposed time-sharing PWM control strategy enables to drive multiple motors simultaneously and independently, with less switching devices than conventional inverters or multi-phase inverters. In addition, power conversion efficiency was calculated from the loss characteristic of the switching devices, and compared with the efficiency of a conventional parallel three-phase inverter.

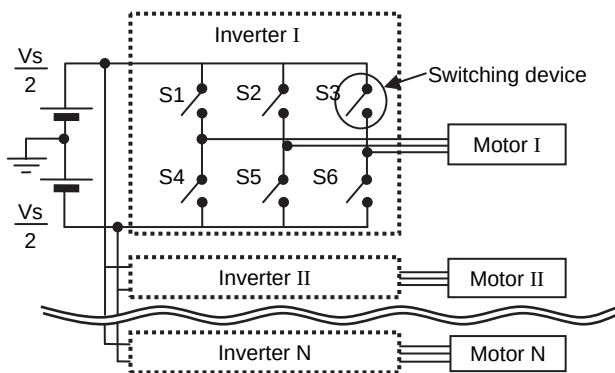
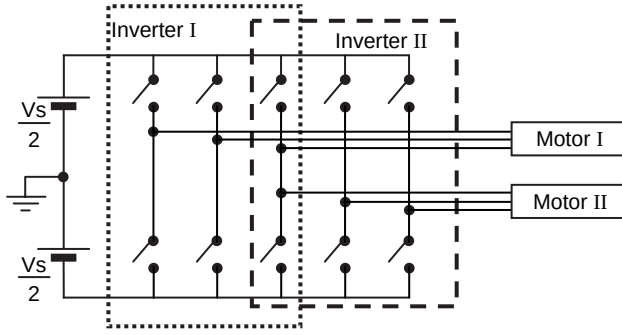
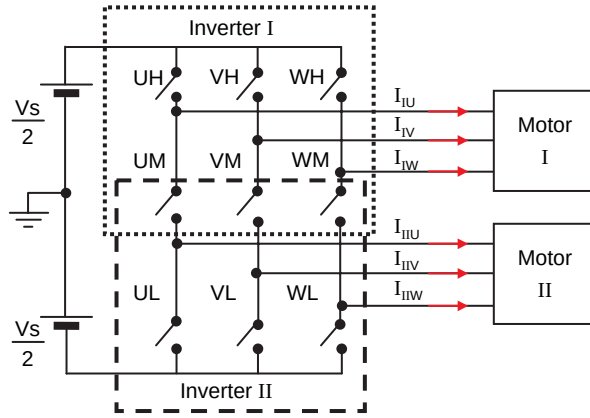


Fig. 1 Multiple-output inverter by parallel 3-phase configuration

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(a) Multiple-output inverter by multi-phase configuration



(b) Multiple-output inverter by multi-level configuration

Fig. 2 Multiple-output inverter

2. PWM Control of a Multiple-output Inverter

2.1. Conventional Inverter

Figure 1 shows the configuration of a conventional three-phase inverter. Each phase of the inverter is formed by two series-connected switching devices on high- and low-side, and three phases (U/V/W) of the inverter are connected in parallel. The motor is driven by controlling the total switching patterns of six switching devices (S1-S6). Figure 3 shows the timing signal (PWM signal) for the ON and OFF states of the U phase switching devices. The signal for each switch is determined by comparing the target voltage waveform, V_u , with the carrier waveform.

2.2. Configuration of Multiple-output Inverter

As Fig. 2 (b) shows, a three-level two-output inverter employs three switching devices (high, middle, and low) for each phase of a three-phase inverter. Inverter I, which drives motor I, consists of the six high- and middle-level switching devices of the three phases (UH, UM, VH, VM, WH, WM). Inverter II consists of the six middle- and low-level switching devices (UM, UL, VM, VL, WM, WL),

and drives motor II. This configuration enables to reduce the number of switching devices that are necessary to control two motors from 12 to 9.

Figure 2 shows examples of control of two-motor system. A conventional inverter and multi-phase inverter need $6 \times N$ switching devices and $4 \times N + 2$ switching devices, respectively. By contrast, a multi-level inverter is able to control N motors using only $3 \times N + 3$ switching devices.

2.3. Proposed Time-sharing PWM Control

Figure 4 shows a control method for each switching device that enables simultaneous independent control of two motors by a three-level, two-output inverter. The figure shows the method for U phase. As shown in Fig. 4 (a), when a three-level two-output inverter is used for simultaneous independent control of two motors, the formerly used carrier cycle, T_s , is divided into two stages, the inverter I control period T_I and the inverter II control period T_{II} . T_I and T_{II} are determined by the ratio between the target voltages V_{IU} and V_{IIU} , and the equations for them are shown in (1) and (2).

$$T_I = T_s \times V_{IU} / (V_{IU} + V_{IIU}) \quad (1)$$

$$T_{II} = T_s \times V_{IIU} / (V_{IU} + V_{IIU}) \quad (2)$$

Carrier waveform I is triangular during period T_I , and has a constant value given by $V_s/2$ during period T_{II} . Carrier waveform II is triangular during period T_{II} , and has a constant value given by $V_s/2$ during period T_I .

Due to the division of the control interval, the average line to line output voltage that is determined by comparison of the target voltage waveform and the carrier waveform is reduced to T_I/T_s for inverter I, and to T_{II}/T_s for inverter II, respectively. Therefore, the voltage waveforms V_{IU}' and V_{IIU}' are determined by multiplying

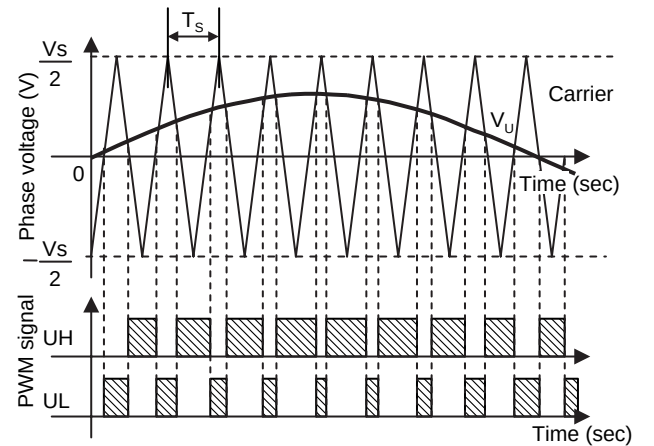


Fig. 3 Conventional PWM control

the target voltage waveforms V_{IU} and V_{IUI} by T_s/T_I and T_s/T_{II} . PWM signals are generated by comparing these V_{IU}' and V_{IUI}' with the carrier waveforms. The relationship between V_{IU}' , V_{IUI}' and V_{IU} , V_{IUI} is expressed by Eqs. (3) and (4).

$$V_{IU}' = V_{IU} \times T_s / T_I \quad (3)$$

$$V_{IUI}' = V_{IUI} \times T_s / T_{II} \quad (4)$$

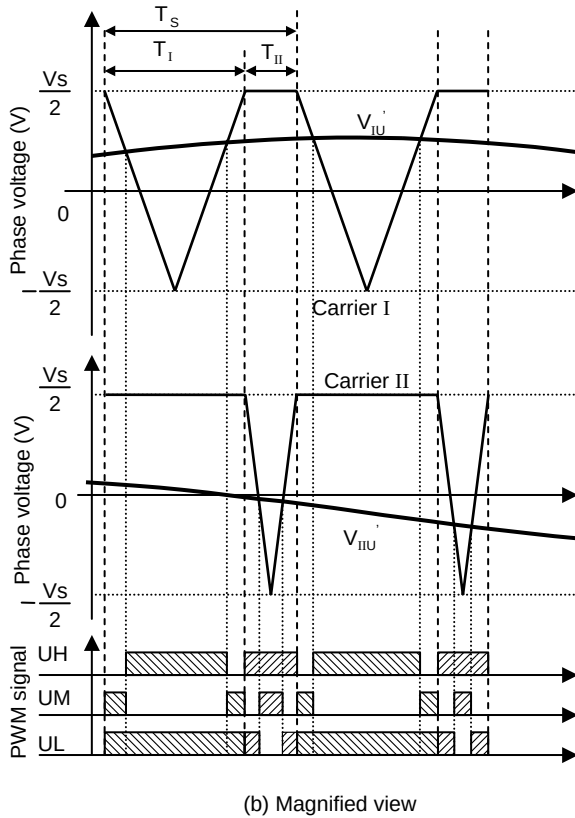
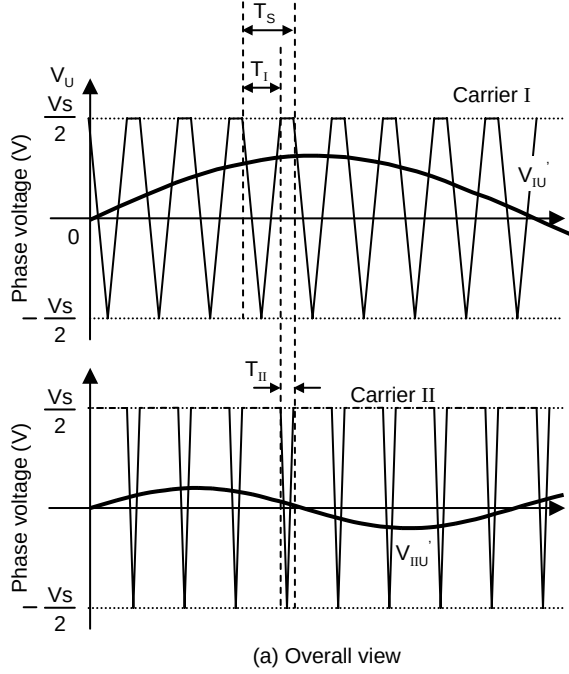


Fig. 4 PWM control in 3-level 2-output inverter

Figure 4 (b) shows the method of generation of the PWM signal during periods T_I and T_{II} for two cycles of the conventional carrier cycle. During period T_I , UH is ON and UM is OFF in the range in which $V_{IU} > \text{carrier I}$, and UH is OFF and UM is ON in the range in which $V_{IU} < \text{carrier I}$. UL is ON for all ranges during period T_I . During period T_{II} , UM is ON and UL is OFF in the range in which $V_{IUI} > \text{carrier II}$, and UM is OFF and UL is ON in the range in which $V_{IUI} < \text{carrier II}$. UH is ON for all ranges during period T_{II} . In the cases of V phase and W phase also, the target voltage waveforms V_{IV} and V_{IW} are compared with carrier waveform I; V_{IIV} and V_{IIW} are compared with carrier waveform II; and control signals are generated in the same way.

Controlling the switching devices using this signal generation method enables motor I to be controlled by inverter I during period T_I , and motor II to be controlled by inverter II during period T_{II} .

Figure 5 (a) shows the current pathway of inverters I and II during period T_I , and Fig. 5 (b) shows the current pathway of the inverters during period T_{II} . Because the low-side switching devices for all phases are ON during period T_I , inverter I is equivalent to a conventional three-phase inverter with respect to motor I. In addition, because the inverter II current flows back into the lower switching devices, which are switched ON, there is no interference between it and the current output of inverter I. In the same

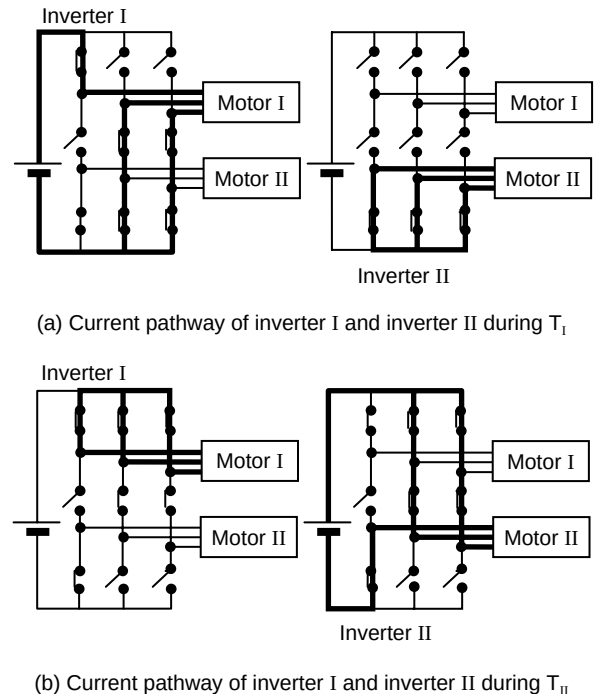


Fig. 5 Current pathway of 3-level 2-output inverter

way, during period T_{II} , inverter II is equivalent to a conventional three-phase inverter with respect to motor II, because the high-side switching devices are switched ON. The inverter I current flows back into the upper switching devices, which are switched ON, and therefore there is no interference between it and the current output of inverter II. This enables motors I and II to be controlled simultaneously and independently. However, the fact that the voltage output of the inverters is zero during the period in which current is flowing back places limitations on the output voltage during control periods T_I and T_{II} . If the average output voltage of inverter I is defined V_I and the average output voltage of inverter II is defined V_{II} , then

$$V_I \leq V_s \times \frac{T_I}{T_s} \quad (5)$$

$$V_{II} \leq V_s \times \frac{T_{II}}{T_s} \quad (6)$$

Given

$$T_I + T_{II} = T_s \quad (7)$$

then

$$V_I + V_{II} = V_s \quad (8)$$

and the range of voltage that can be output by V_I and V_{II} is as shown in Fig. 6.

2.4. Reduction of Switching Times

Using the method of generation of PWM signals shown in Fig. 4, switching devices are switched ON or OFF a total of seven times for each carrier period T_s (UH: twice; UM: four times; UL: once). The number of instances of switching has increased from four for a conventional parallel three-phase inverter. This is a factor in increased switching loss. To reduce switching times for each carrier period, PWM generation method by a sawtooth waveform is proposed. As shown in Fig. 7, switching devices are turned on and off only 3 times for each carrier period (UH: once; UM: once; UL: once). Substantial reduction of total switching times can be realized by using PWM generation with sawtooth waveform.

3. Simulation and Analysis Results

3.1. Analysis Method

An electric circuit simulation was conducted in order to verify the viability of the proposed time-sharing PWM control for a multiple-output inverter. Ideal switching devices (switching time: 0 sec; resistance: 0 Ω) were used in this simulation. PSIM was employed as the electric

circuit simulator. The control logic used in the simulation is shown in Fig. 8. The PWM signals UH (VH, WH), UM (VM, WM) and UL (VL, WL) were determined by comparing voltage waveforms V_{IU} (V_{IV} , V_{IW}), V_{IIU} (V_{IIV} , V_{IIW}) and the carrier waveforms in periods T_I and T_{II} , respectively.

3.2. Output Voltage Characteristic

Figure 9 shows the three-phase output current waveform for a three-level two-output inverter during steady-state operation. The frequency and amplitude of the output current are 100 Hz and 50 A, respectively, for inverter I, and 300 Hz and 20 A, respectively, for inverter

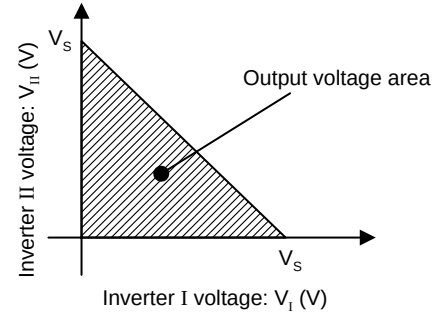


Fig. 6 Output voltage area of 3-level 2-output inverter

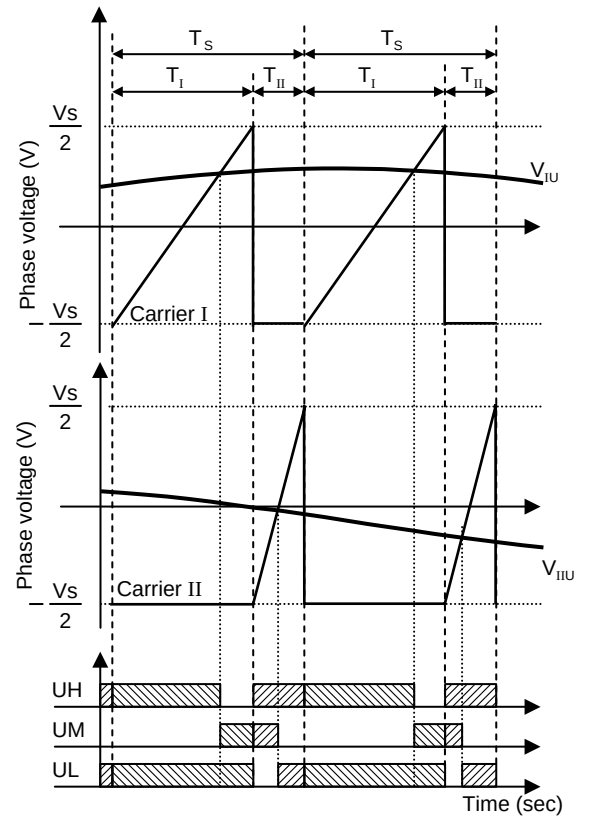


Fig. 7 Enhanced PWM control in 3-level 2-outputs inverter

II in this multi-level system. This indicates that current for two motors can be controlled simultaneously and independently.

Figure 10 shows the transient response of the three-phase current waveforms of three-level two-output inverter. The results show that the system is able to respond to the command value, changing the frequency of the output current of inverter I from 200 to 400 Hz, and the amplitude of the output current of inverter II from 25 A to 50 A.

3.3. Power Conversion Efficiency Characteristic

Figure 11 shows the power conversion efficiency characteristic of the three-level, two-output inverter using

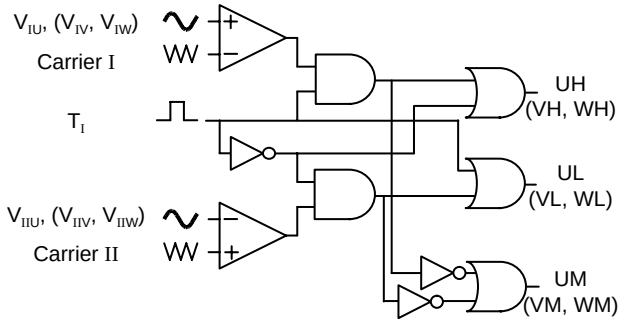


Fig. 8 3-level 2-output inverter control logic

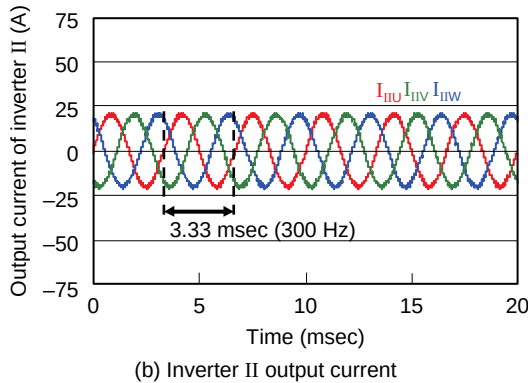
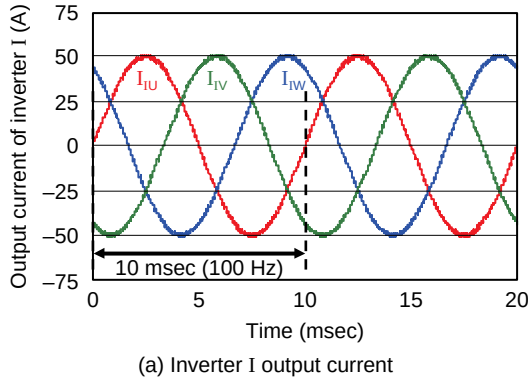


Fig. 9 Steady-state operation of 3-level 2-output inverter

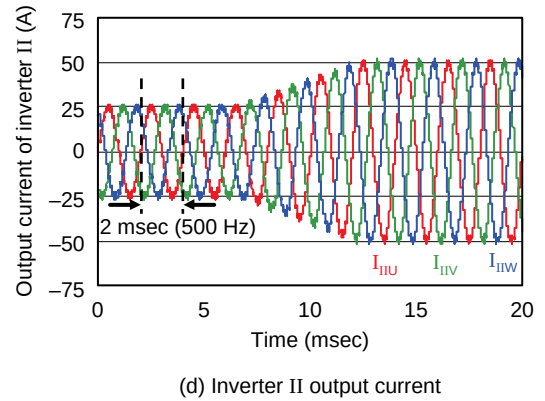
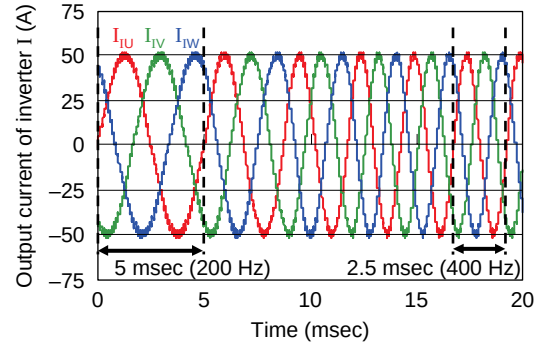
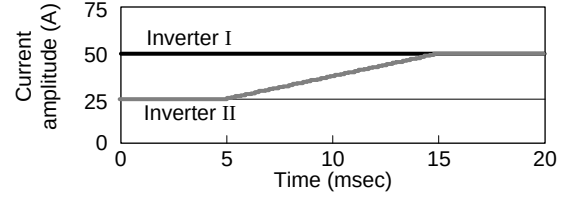
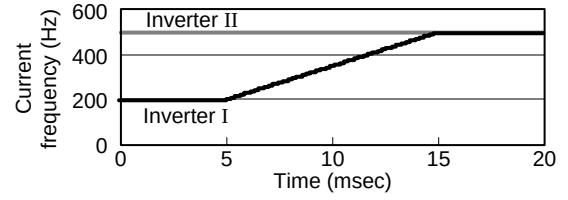
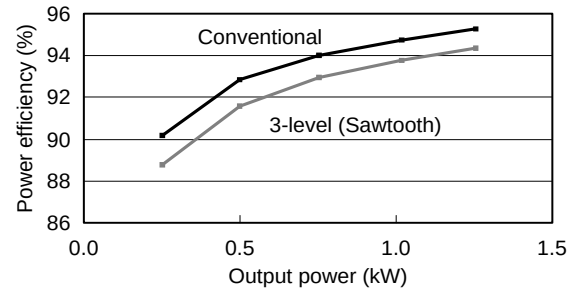


Fig. 10 Transient characteristic of 3-level 2-outputs inverter



sawtooth-wave PWM control and a conventional two-parallel two-output inverter. Figure 12 shows the results of a power loss analysis for both inverters at 1 kW. MOSFET (100 V, 75 A) were used as the switching devices in this analysis of power conversion efficiency. Both switching loss (ON loss and OFF loss) and conduction loss ($I_D \times V_{DS}$, $I_S \times V_{SD}$) were taken into consideration. A DC source voltage of $V_s = 48$ V and a motor speed of 1000 rpm were set as the operating conditions for the inverter. Phase and amplitude were identical for motors I and II. Switching loss was calculated from the switching loss characteristic in relation to voltage and current, and conduction loss was calculated from the ON voltage characteristic in relation to the current.

Figure 11 shows that the power conversion efficiency of the new inverter is lower than that of the conventional inverter across the entire operating power range. The results of the analysis of power loss in Fig. 12 indicate that conduction loss is the main factor in the lower power efficiency of the new inverter since there was an increase of 0.8 W in switching loss and 9.8 W in conduction loss for the proposed inverter. Three-level two-output inverter indicates increased conduction loss, because it employs a larger number of switching devices in the current pathways than a conventional inverter (three devices as opposed to two). The phase currents for two motors pass through each switching devices at the same time. Therefore the switching loss increases by 0.8 W despite the reduction in the amount of switching.

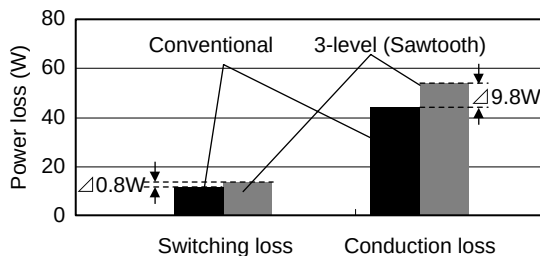


Fig. 12 Power loss analysis of 2-output inverter

4. Conclusion

The research discussed in this paper proposed a previously unconsidered form of PWM control that enables to drive multiple motors simultaneously and to reduce the amount of switching devices. The viability of this form of control was demonstrated by a simulation analysis. The results of this verification showed that the frequency and amplitude of the three-phase output current could be controlled independently for each motor, demonstrating the validity of the new system. However, the analysis indicated that there are also limitations on

output voltage in multi-level inverters like multi-phase inverters. The carrier waveform was converted to a sawtooth wave in order to reduce the amount of switching, and an analysis showed that switching loss was similar to that of a conventional inverter. The analysis results of power conversion efficiency showed that the increase in the number of switching devices in the current pathways had resulted in an increase in conduction loss and that switching devices with good conduction loss characteristics would be suitable for use with this method. A current phase difference between inverters I and II affects conduction loss. Adjusting the current phase difference may be necessary to enhance efficiency.

References

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