HONDA RENESAS

News Release

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Honda and Renesas Sign Agreement to Develop High-Performance SoC for Software-Defined Vehicles -Delivering Industry-Leading AI Performance and Power Efficiency for the Honda 0 Series in the Late 2020s-

TOKYO, Japan, January 8, 2025 — Honda Motor Co., Ltd. (TSE: 7267) and Renesas Electronics Corporation (TSE:6723) announced today that they have signed an agreement to develop a high-performance system-on-chip (SoC) for software-defined vehicles (SDVs). The new SoC is designed to deliver leading-edge*1 AI performance of 2,000*2 TOPS combined with a world-class power efficiency of 20 TOPS/W, and is slated for use in future models of the "Honda 0 (Zero) Series," Honda's new electric vehicle (EV) series, specifically those that will be launched in the late 2020s. The agreement was announced during a Honda press conference held at CES 2025 in Las Vegas, Nevada on January 7.

Honda is developing original SDVs to provide a mobility experience optimized for each individual customer in the Honda 0 Series. The Honda 0 Series will adopt a centralized E/E architecture that combines multiple electronic control units (ECUs) responsible for controlling vehicle functions into a single ECU. The core ECU, which serves as the heart of the SDV, manages essential vehicle functions such as Advanced Driver Assistance Systems (ADAS) and Automated Driving (AD), powertrain control, and comfort features, all on a single ECU. To achieve this, the ECU requires a SoC that provides higher processing performance than traditional systems, while minimizing any increase in power consumption.

Renesas is committed to providing automotive semiconductor solutions that enable automobile OEMs to develop SDVs. Renesas' R-Car solutions offer higher AI performance with the ability to customize by leveraging multi-die chiplet technology*3 and integrating AI accelerators*4 into its SoC.

To realize the Honda vision for SDVs, Honda and Renesas reached an agreement to develop a high-performance SoC compute solution designed for core ECUs. Using TSMC's leading-edge 3-nm automotive process technology, this SoC also can achieve a significant reduction in power consumption. Additionally, it realizes a system that utilizes multi-die chiplet technology to combine Renesas' generic fifth-generation (Gen 5) R-Car X5 SoC series with an AI accelerator optimized for AI software developed independently by Honda. With this combination, the system aims to achieve one of the industry's top class AI performances with power efficiency. The SoC chiplet solution will provide the AI performance required for advanced functions such as AD, while keeping power consumption low. Chiplet technology allows flexibility to create customized solutions and offers future upgrades for functional and performance improvements.

Honda and Renesas have collaborated closely for many years. This agreement will accelerate the integration of advanced semiconductor and software innovations into the Honda 0 Series, enhancing the mobility experience for customers.

*1 Renesas estimate as of January 2025

*2 Tera Operations Per Second (TOPS) is a metric of AI processing performance and measures the number of operations that can be performed per second. Based on a sparse AI model.

*3 Technology to build a system by combining multiple chips with different functions

*4 Hardware designed for high-speed and high-efficiency AI (artificial intelligence) computational processing